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(54) Multi-chip module.

(57) A multi-chip module includes a base board (30), a thin-film multi-layer circuit board (32) which is provided on a first surface of the base board and has a multi-layer structure in which insulating layers and wiring conductors are stacked, circuit elements (32A-5) mounted on a main surface of the thin-film multi-layer circuit board, and terminals (34) which are attached to the main surface of the thin-film multilayer circuit board and electrically connect the wiring conductors to circuits formed on a wiring board on which the multi-chip module is mounted.

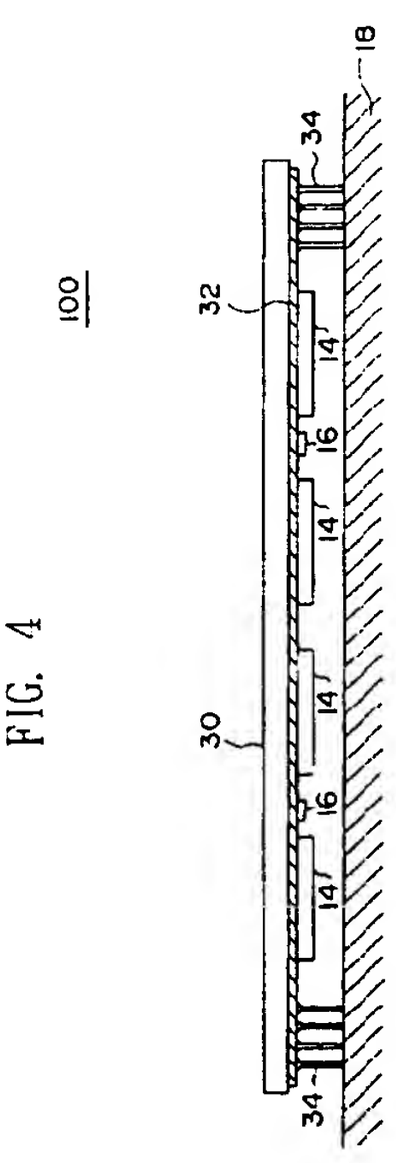

FIG. 4

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BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to a multi-chip module in which a plurality of circuit elements such as LSI chips are mounted on a high-density wiring board (also referred to as a circuit board).

Recently, multi-chip modules have become attractive in which a plurality of LSI chips are mounted on a high-density wiring board in order to speed up the operation and reduce the production cost. As is well known, multi-chip modules are classified into three types, namely a MCM-L, MCM-C and MCM-D. The multi-chip modules of the MCM-L type have a printed wiring board on which circuit elements are mounted, and enable reduction in the production cost. The multi-chip modules of the MCM-C type have a thin-film multilayer ceramic board on which circuit elements are mounted, and enable reduction in the production cost and speeding up the operation to some extent. The multi-chip modules of the MCM-D type have a thick-film board made of ceramic or the like, on which a circuit board having at least one multi-layer structure in which an insulating layer and at least one wiring conductor layer are alternately stacked. Circuit elements are mounted on the above circuit board. As compared to the other two types, the MCM-D type multi-chip modules operate at high speeds and enable mounting of circuit elements with a high density.

Fig. 1 is a side view of a conventional MCM-D type multi-chip module, which includes a thick-film ceramic board 10 having a multi-layer structure. LSI chips 14 and passive elements 16 such as resistors and capacitors are mounted on a first surface of the thick-film ceramic board 10. These circuit elements 14 and 16 are connected to wiring lines formed inside the thick-film ceramic board 10. A large number of I/O pins 12 are attached to a second surface of the ceramic board 10 opposite to the first surface thereof. The multi-chip module is directly mounted on a printed wiring board 18 by inserting the I/O pins 12 into holes formed in the printed wiring board 18.

Fig. 2 is a side view of a conventional MCM-D type multi-chip module. In Fig. 2, parts that are the same as those shown in Fig. 1 are given the same reference numbers as previously. In order to speed up the operation and increase the density, a thin-film circuit board 20 is provided on the first surface of the thick-film ceramic board 10. The circuit elements 14 and 16 are mounted on the thin-film circuit board 20, and are connected to the thick-film ceramic board 10 and the I/O pins 12 via wiring lines of the thin-film circuit board 20. On the opposite surfaces of the boards 10 and 20, are provided pads (illustration thereof is omitted) for connections, whereby the wiring lines of the boards 10 and 20 are electrically connected together. The multi-chip module shown in Fig. 2 is directly mounted on the printed wiring board 18 by means of the I/O pins 12 in the same manner as the multi-chip module shown in Fig. 1.

Fig. 3 is a side view of a conventional MCM-D type multi-chip module. In Fig. 3, parts that are the same as those shown in Fig. 2 are given the same reference numbers as previously. The thin-film circuit board 20 is mounted on a base board 24 which does not have a wiring conductor layer. The base board 24 is made of ceramic, a silicon wafer or a metallic material such as aluminum. The base board 24 is provided in a base board mounting package 22. The package 22 is made of ceramic or mold resin, and a recess portion in which the base board 24 is accommodated. I/O pins 28 are attached to peripheral portions of the package 22 along the edges thereof. The thin-film circuit board 20 and the I/O pins 28 are connected by wires 26. Pads (not shown) for bonding the wires 26 are provided on the package 22. The multi-chip module shown in Fig. 3 is mounted on the printed wiring board 18 by means of the I/O pins 28. In the structure shown in Fig. 3, the circuit elements 14 and 16 face the printed wiring board 18.

However, the above-mentioned conventional multi-chip modules shown in Figs. 1 through 3 have the following disadvantages.

The thick-film ceramic board 10 used in the multi-chip module shown in Fig. 1 has a wiring conductor formation density lower than that of the thin-film circuit board 20 shown in Fig. 2. Hence, a large number of stacked layers is needed to form wiring lines which realize a desired circuit configuration. Further, th larger the number of stacked layers, the longer the wiring lines. This delays transmission of signals. Hence, the structure shown in Fig. 1 is not suitable for circuit configurations particularly needed to operate at high speeds.

The multi-chip module shown in Fig. 2 utilizes the thick-film ceramic board 10 and the thin-film circuit board 20, and hence has a high production cost. The process of forming the thin-film circuit board 20 greatly depends on the surface condition (warp, roughness, pore and so on) of the ceramic part of the thick-film ceramic board 10 as well as the wiring lines (pad parts) exposed from the ceramic part. Hence, a defect will occur in the thin-film circuit board 20 and a high yield cannot be obtained if the thick-film ceramic board 10 does not have a good surface condition.

The multi-chip module shown in Fig. 3 is advantageous due to use of the base board 24 made of bulk ceramic, silicon wafer or a metallic material such as aluminum because the base board 24 can be less expensive and has a good surface condition. However, the multi-chip module shown in Fig. 3 needs the package 22 necessary to mount the multi-chip module on the printed wiring board. The use of the package 22 increases the production cost. Further, if the package

22 does not have good electrical characteristics, signals output from the multi-chip module will be delayed or contain a noise component. These phenomena degrade the performance of the multi-chip module. If there is a demand for an increased number of I/O pins 28 and/or an increased number of circuit elements mounted to the base board 24 due to a modification of the circuit configuration or the like, the package 22 needs to be redesigned. This leads to an increase in the production cost and the time necessary for redesign and reproduction.

Further, the structures shown in Figs. 1 through 3 have a common disadvantage in that the thick-film ceramic board 10 and the base board mounting package 22 need to be redesigned each time the shape of the multi-chip module is modified. This increases the turnaround time of the multi-chip module design and production as well as the production cost.

SUMMARY OF THE INVENTION

It is a general object of the present invention to provide a multi-chip module in which the above disadvantages are eliminated.

A more specific object of the present invention is to provide a less-expensive, high-density, high-speed multi-chip module having high flexibility in the design and production.

The above objects of the present invention are achieved by a multi-chip module comprising: a base board; a thin-film multi-layer circuit board which is provided on a first surface of the base board and has a multi-layer structure in which insulating layers and wiring conductors are stacked; circuit elements mounted on a main surface of the thin-film multi-layer circuit board; and terminals which are attached to the main surface of the thin-film multi-layer circuit board and electrically connect the wiring conductors to circuits formed on a wiring board on which the multi-chip module is mounted.

According to the present invention, since the terminals for external connections are attached to the thin-film multi-layer circuit board, the base board supporting the thin-film multi-layer circuit board does not need wiring conductors unlike the base board mounting package used in the prior art, whereby less-expensive multi-chip modules having good operation characteristics can be produced. Further, the multi-chip module according to the present invention has a high degree of flexibility in design modifications. That is, the design of the multi-chip module can be modified by changing the thin-film multi-layer structure. Further, a modification of the shape of the multi-chip modul can be easily achieved by changing the shape of only the thin-film multi-layer circuit board. Hence, it is possible to greatly reduce the TAT of the design and production of the multi-chip module and the production cost.

BRIEF DESCRIPTION OF THE DRAWINGS

Other objects, features and advantages of the present invention will become more apparent from the following detailed description when read in conjunction with the accompanying drawings, in which:

Fig. 1 is a side view of a first conventional multi-chip module;

Fig. 2 is a side view of a second conventional multi-chip module;

Fig. 3 is a side view of a third conventional multi-chip module;

Fig. 4 is a side view of a multi-chip module according to a first embodiment of the present invention;

Fig. 5 is a cross-sectional view of an essential part of the multi-chip module shown in Fig. 4;

Fig. 6 is a perspective view of the multi-chip module shown in Fig. 4 viewed from the bottom thereof;

Fig. 7 is a perspective view of multi-chip modules according to the first embodiment of the present invention on a printed wiring board;

Fig. 8 is a side view of a multi-chip module according to a second embodiment of the present invention;

Fig. 9 is a side view of a multi-chip module according to a third embodiment of the present invention;

Fig. 10 is a side view of a multi-chip module according to a fourth embodiment of the present invention;

Fig. 11 is a side view of the multi-chip module shown in Fig. 4 with a cover made of resin;

Fig. 12 is a side view of the multi-chip modul shown in Fig. 4 with a cover formed with a lid;

Fig. 13 is an exploded perspective view of th multi-chip module shown in Fig. 12 with a cooling structure;

Fig. 14 is a perspective view of the multi-chip module shown in Fig. 12 with a cooling structure attached thereto; and

Fig. 15 is a side view showing cooling structures that can be applied to the present invention multi-chip module.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

A description will now be given, with reference to Figs. 4 and 5, of a multi-chip module 100 according to a first embodiment of the present invention. Fig. 4 is a side view of the multi-chip module 100, and Fig. 5 is a cross-sectional view of an essential part of the multi-chip module 100 shown in Fig. 4. The multi-chip module 100 shown in Figs. 4 and 5 is of a PGA (Pin Grid Array) type, and includes a base board 30 and a thin-film multi-layer circuit board 32, which is provid-

ed on a surface of the base board 30 facing the printed wiring board 18.

As shown in Fig. 5, the thin-film multi-layer circuit board 32 has a multi-layer structure, which is made up of a first wiring conductor 32A-1, a second wiring conductor 32A-2, a third wiring conductor 32A-3, a fourth wiring conductor 32A-4, a fifth wiring conductor 32A-5, a first insulating layer 32B-1, a second insulating layer 32B-2, a third insulating layer 32B-3, a fourth insulating layer 32B-4 and a fifth insulating layer 32B-5. These conductors and insulating layers are serially stacked on the base board 30 in the order shown in Fig. 5. The first wiring conductor 32A-1 is provided on the base board 30.

The fifth wiring conductor 32A-5 functions as pads used to attach I/O pins 34 and LSI chips 14 thereto. The pads 32A-5 to which the I/O pins 34 are attached are arranged in an array. The wiring conductors 32A-1 through 32A-4 extend in the longitudinal and lateral directions (X and Y directions) in the thin-film multi-layer board 32. The wiring conductors located at the different layer levels are electrically connected together by means of a conductor formed in a via hole formed in the insulating layer sandwiched between those wiring conductors. For example, the wiring conductor 32A-1 is connected to the wiring conductor 32A-2 via a via hole 36 formed in the insulating layer 32B-1. The wiring conductor 32A-1 is, for example, a power supply layer.

The thin-film multi-layer circuit board 32 having the above-mentioned multi-layer structure can be produced by a conventional LSI production process.

The attachment surface of the pads 32A-5 is exposed from the insulating layer 32B-5. The I/O pins 34 are attached to the pads 32A-5 by solder 38. The areas of the pads 32A-5 exposed from the insulating layer 32B-5 are greater than those of attachment parts 34a of the I/O pins 34. In the structure shown in Fig. 5, the wiring conductor 32A-1 serving as the power supply layer is connected, via a via hole, to the I/O pin 34 located on the left side of the drawing. The first embodiment of the present invention has an essential feature such that the I/O pins 34 inserted into the printed wiring board 18 are attached to the thin-film multi-layer wiring board 32. Soldering of the I/O pins 34 can be performed in a conventional manner.

The LSI chip 14 shown in Fig. 15 is attached to the pad 32A-5 by means of a solder bump 40. Instead of the solder bump 40, a wire bonding or a TAB (Tape Automated Bonding) lead can be used.

A description will now be given of the materials of the parts of the multi-chip module shown in Figs. 4 and 5. The base board 30 is made of a ceramic such as AlN, Al_2O_3 or Mulite, a metallic material such as Al, Cu, a Cu-W alloy or the like, Si or glass. The base board 30 may be formed of resin used as an insulating material for conventional printed wiring boards, such as glass epoxy or glass polyimide.

The insulating layers 32B-1 through 32B-5 of the thin-film multi-layer circuit board 32 are made of an organic material such as polyimide, Teflon (trademark), or epoxy. The wiring conductors 32A-1 through 32A-5 are made of Al, Cu or the like.

The thin-film multi-layer circuit board 32 is not limited to the structure shown in Fig. 5, but can be a stacked structure in which arbitrary numbers of wiring conductors and insulating layers are alternately stacked.

Fig. 6 is a perspective view of the multi-chip module 100. The I/O pins 34 are arranged in the peripheral areas of the thin-film multi-layer circuit board 32 so as to surround the LSI chips 14 and the passive elements 16 such as resistors and capacitors. For the sake of simplicity, the illustration of the I/O pins 34 is simplified. On the surface of the base board 30 opposite to the surface having the thin-film multi-layer circuit board 30 is provided a fin-type heat sink 42 for cooling the multi-chip module 100. The heat sink 42 may have a pipe (not shown) in which coolant water flows.

Fig. 7 is a perspective view of multi-chip modules 100 which are mounted on the printed wiring board 18. The multi-chip modules 100 are mounted on a mounting surface of the printed wiring board 18 together with semiconductor elements 46. A cooling air stream 44 is present, as indicated by the arrows shown in Fig. 7.

Fig. 8 is a side view of a multi-chip module 100A according to a second embodiment of the present invention. In Fig. 8, parts that are the same as thos shown in the previously described figures are given the same reference numbers as previously. The multi-chip module 100A shown in Fig. 8 is of a FLT (flat) package type. I/O pins 50 are formed with gull-wing type leads, and are soldered to the pads 32A-5 shown in Fig. 5. The multi-chip module 100A shown in Fig. 8 has the same advantages as the first embodiment of the present invention. However, the number of attachable I/O pins 50 is less than that of I/O pins 34 of th PGA type. A cooling structure can be applied to the multi-chip module 100A in the same manner as that used in the first embodiment of the present invention. The I/O pins 50 may be TAB leads.

Fig. 9 is a side view of a multi-chip module 100B according to a third embodiment of the present invention. In Fig. 9, parts that are the same as those shown in the previously described figures are given the same reference numbers as previously. The multi-chip module shown in Fig. 9 is of a leadless type such as a BGA (Ball Grid Array) or a LGA (Land Grid Array). Solder bumps 52 are attached to the pads 32A-5 shown in Fig. 5. For the sake of simplicity, two bumps 52 are respectively shown on the left and right side of the figure. However, bumps 52 can be arranged in an array as in the case of the PGA type. Th multi-chip module 100B shown in Fig. 9 has the same advantag-

es as the first embodiment of the present invention. In the LGA type, flat pads are used instead of the bumps 52. A cooling structure can be employed in the same manner as that used in the first embodiment of the present invention.

Fig. 10 is a side view of a multi-chip module 100C according to a fourth embodiment of the present invention. In Fig. 10, parts that are the same as those shown in the previously described figures are given the same reference numbers as previously. The multi-chip module 100C shown in Fig. 10 is of a wire bonding type. Wires 54 are bonded to the pads 32A-5 shown in Fig. 5. The multi-chip module 100C is directly placed on and in contact with the printed wiring board 18. This mounting is different from the mounting according to the first through third embodiments of the present invention. The fourth embodiment of the present invention cannot employ a cooling structure similar to that used in the first through third embodiments of the present invention. The multi-chip module 100C is cooled via the printed wiring board 18.

The I/O terminals of the present invention are not limited to the above-mentioned types, and other types of I/O terminals can be used.

Fig. 11 is a side view of the multi-chip module 100 to which a cover 56 made of resin is attached. The cover 56 is provided so that it seals the LSI chips 14 and the circuit elements 16. The resin cover 56 is made of, for example, epoxy-based resin or a silicon-based resin (potting). The resin cover 56 can be provided so that it seals only some of the LSI chips 14 and the circuit elements 16. The cover 56 can be applied to the second through fourth embodiments of the present invention in the same manner as described above.

Fig. 12 is a side view of the multi-chip module 100 to which a lid 58 is attached. Figs. 13 and 14 are perspective views of the structure shown in Fig. 12 with the heat sink 42 shown in Fig. 6. The lid 58 is attached to the thin-film multi-layer circuit board 32 via a ring-shaped seal member 60 (Fig. 13). In the structure shown in Figs. 12 and 13, the lid 58 seals all the LSI chips 14 and other circuit elements 16. As shown in Fig. 13, recesses 58a are formed in the lid 58 to reinforce the lid 58 itself. A heat conducting member may be provided between the recesses 58a and the LSI chips 14 in order to radiate heat generated by the LSI chips 14. It is possible to use a lid which seals only some LSI chips 14 and circuit elements 16. The lid 58 is made of, for example, a metallic material such as aluminum or covar or a resin.

The cooling structures which can be applied to the multi-chip module of the present invention are not limited to the aforementioned heat sink 42, but other appropriate cooling structures can be attached to the base board 30. For example, as shown in Fig. 15, it is possible to use a fin-type heat sink (of an air cooling type or a water cooling type) 62, a cold plate (of a water cooling type) 64 or a built-in Peltier-effect plate 66 alone or any combinations thereof. If the strength of the base board 30 becomes weak because of attachment of the cooling structure, a conventional supporting member may be used to mount the multi-chip module on the printed wiring board 18.

According to the present invention, since the I/O terminals for external connections are attached to the thin-film multi-layer circuit board, the base board supporting the thin-film multi-layer circuit board does not need wiring conductors unlike the base board mounting package used in the prior art, whereby less-expensive multi-chip modules having good operation characteristics can be produced. Further, the multi-chip module according to the present invention has a high degree of flexibility in design modifications. That is, the design of the multi-chip module can be modified by changing the thin-film multi-layer structure. Further, a modification of the shape of the multi-chip module can be easily achieved by changing the shape of only the thin-film multi-layer circuit board. Hence, it is possible to greatly reduce the TAT of the design and production of the multi-chip module and the production cost.

The present invention is not limited to the specifically disclosed embodiments, and variations and modifications may be made without departing from the scope of the present invention.

Claims

1. A multi-chip module comprising:

   a base board (30);

   a thin-film multi-layer circuit board (32) which is provided on a first surface of the bas board and has a multi-layer structure in which insulating layers and wiring conductors are stacked;

   circuit elements (32A-5) mounted on a main surface of the thin-film multi-layer circuit board; and

   terminals (34) which are attached to the main surface of the thin-film multi-layer circuit board and electrically connect the wiring conductors to circuits formed on a wiring board on which the multi-chip module is mounted.

2. The multi-chip module as claimed in claim 1, characterized in that said terminals comprise lead members.

3. The multi-chip module as claimed in claim 1, characterized in that said terminals comprise leadless members.

4. The multi-chip module as claimed in claim 1, 2 or 3, characterized in that said terminals are sol-

dered to wiring conductors of the thin-film multi-layer circuit board facing the wiring board, so that the terminals are supported by the thin-film multilayer circuit board.

5. The multi-chip module as claimed in any of claims 1 to 4, characterized in that wiring conductors of the thin-film multi-layer circuit board facing the wiring board comprise pad areas to which said terminals are connected.

6. The multi-chip module as claimed in claim 2, characterized in that said lead members comprise lead pins vertically extending from the main surface of the thin-film multi-layer circuit board.

7. The multi-chip module as claimed in claim 2, characterized in that said lead members comprise flat-type lead pins.

8. The multi-chip module as claimed in claim 2, characterized in that said lead members comprise wire leads.

9. The multi-chip module as claimed in claim 2, characterized in that said lead members comprise tape-automated bonding leads.

10. The multi-chip module as claimed in any of claims 1 to 5, characterized in that said terminals are located in peripheral areas on the main surface of the thin-film multi-layer circuit board so that said terminals surround the circuit elements.

11. The multi-chip module as claimed in any of claims 1 to 5 or claim 10, characterized by further comprising a cover which is formed on the main surface of the thin-film multi-layer circuit board and covers the circuit elements.

12. The multi-chip module as claimed in any of claims 1 to 5 or claims 10 or 11, characterized by further comprising a cooling structure which is formed on a second surface of the base board opposite to the first surface thereof and which cools the multi-chip module.

FIG. 1 PRIOR ART

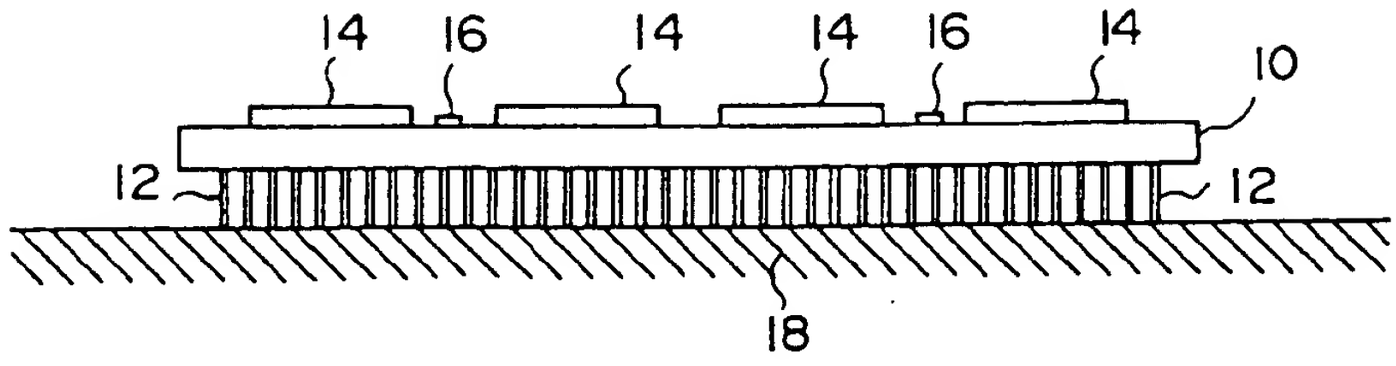


FIG. 2 PRIOR ART

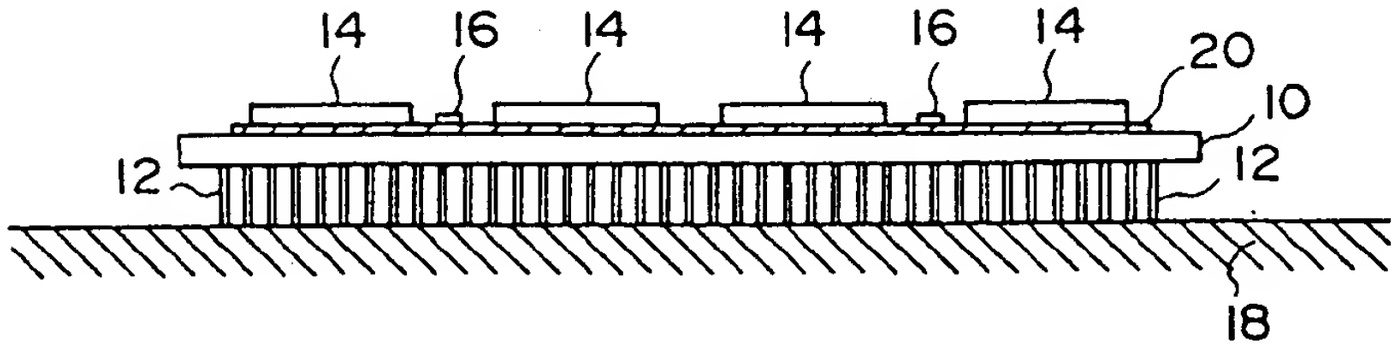


FIG. 3 PRIOR ART

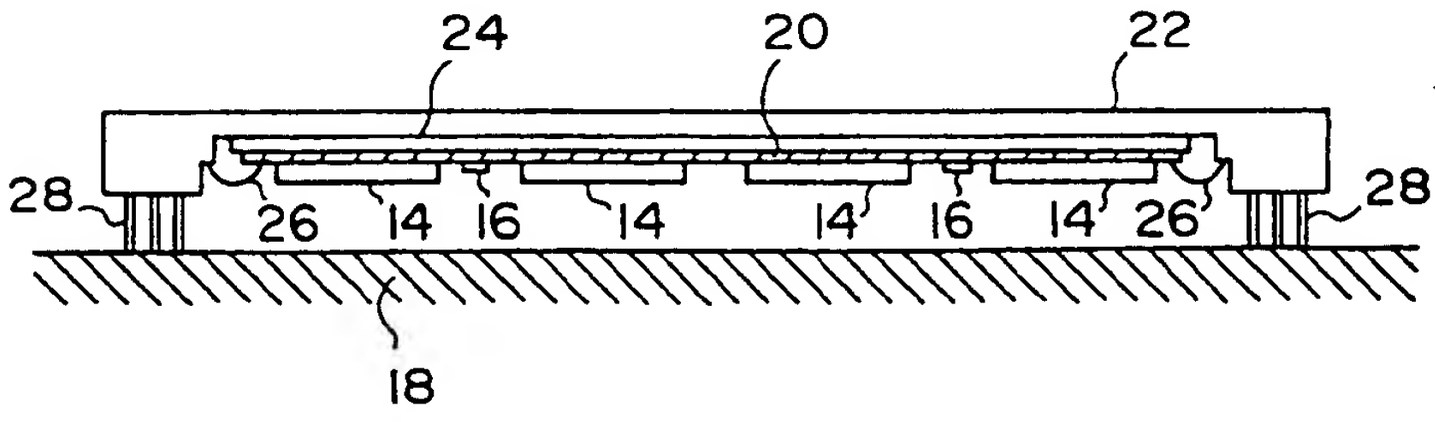


FIG. 4

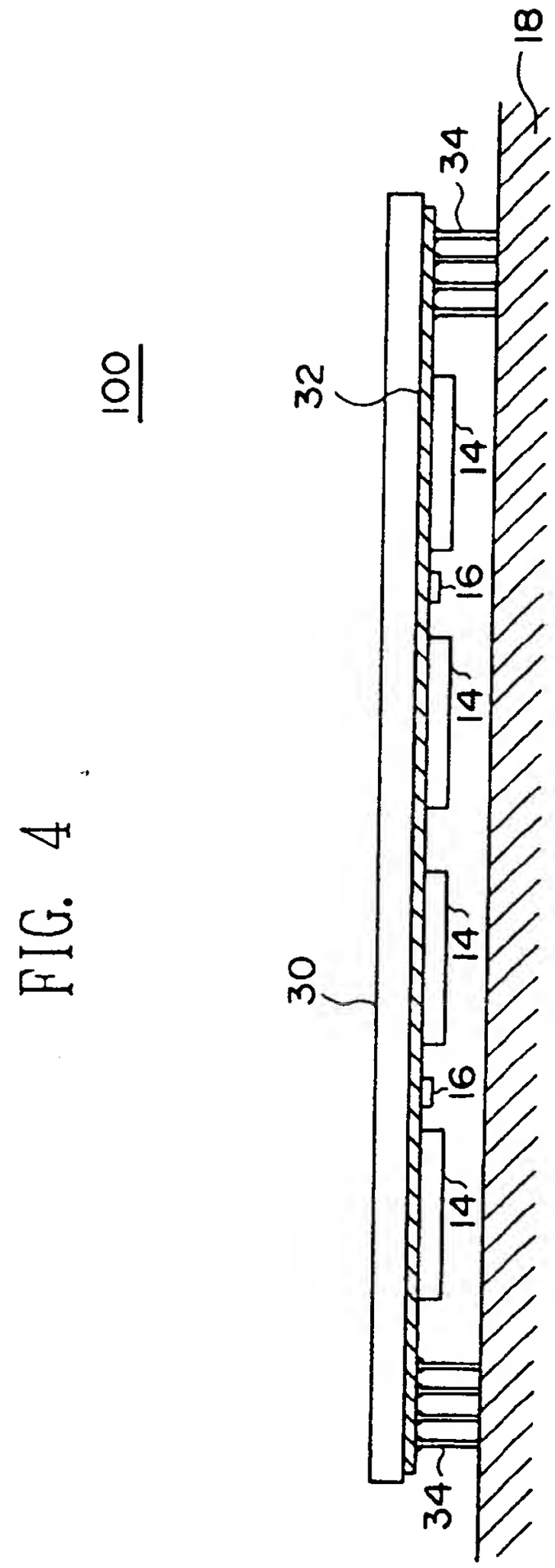


FIG. 5

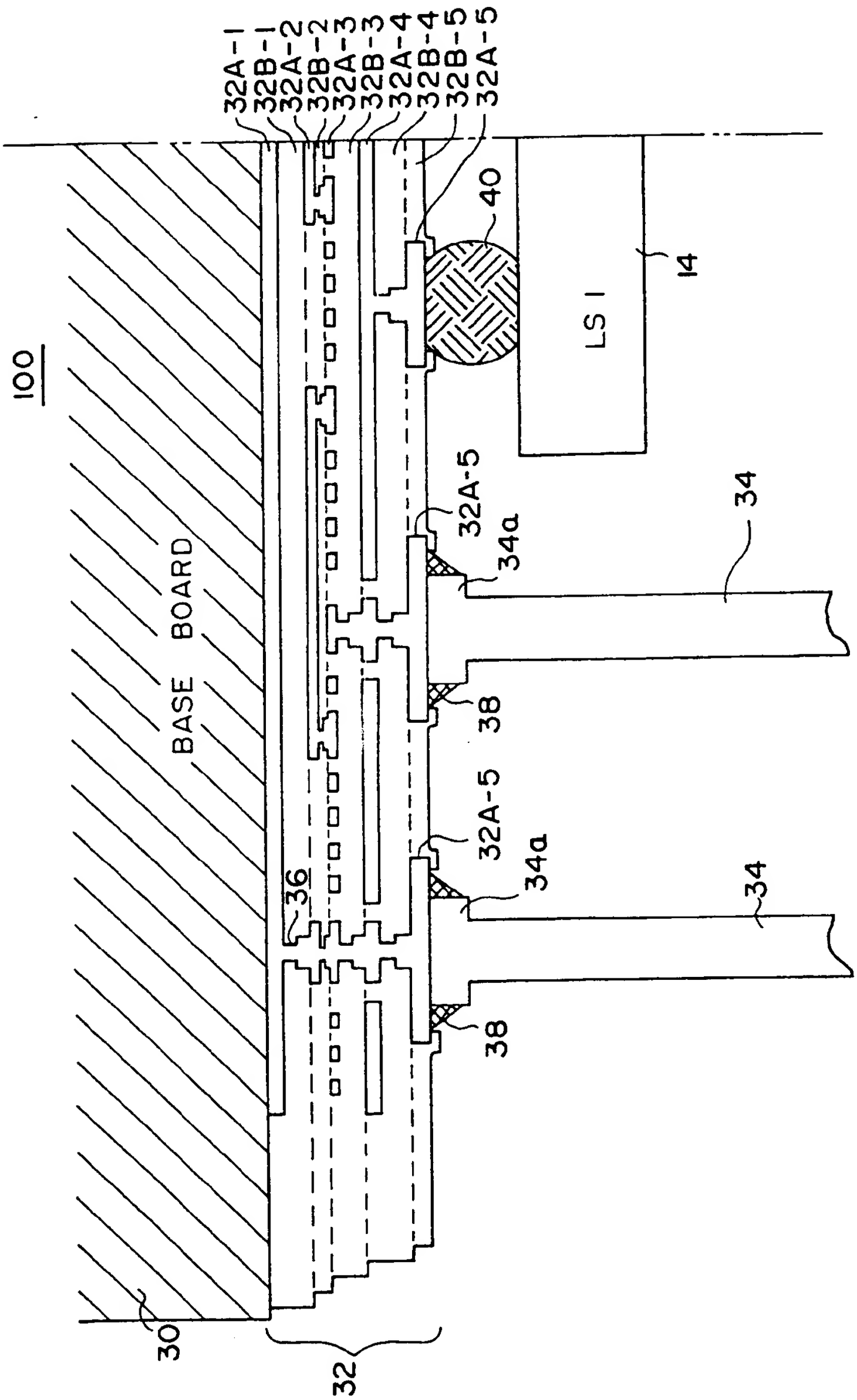

32A-1
32B-1
32A-2
32B-2
32A-3
32B-3
32A-4
32B-4
32B-5
32A-5
40
14
LS I
100
BASE BOARD
32A-5
34a
34
38
32A-5
34a
34
38
36
30
32

FIG. 6

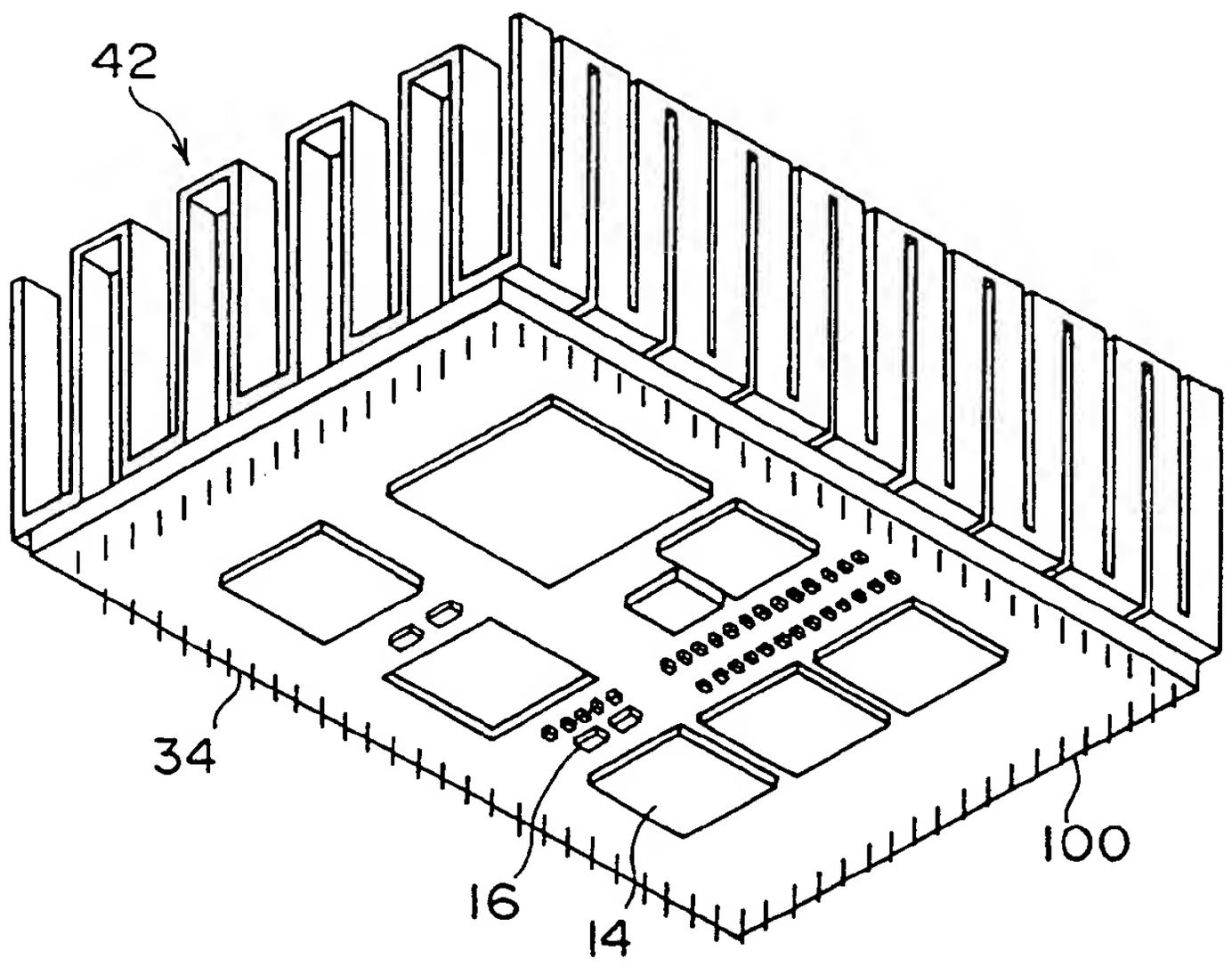


FIG. 7

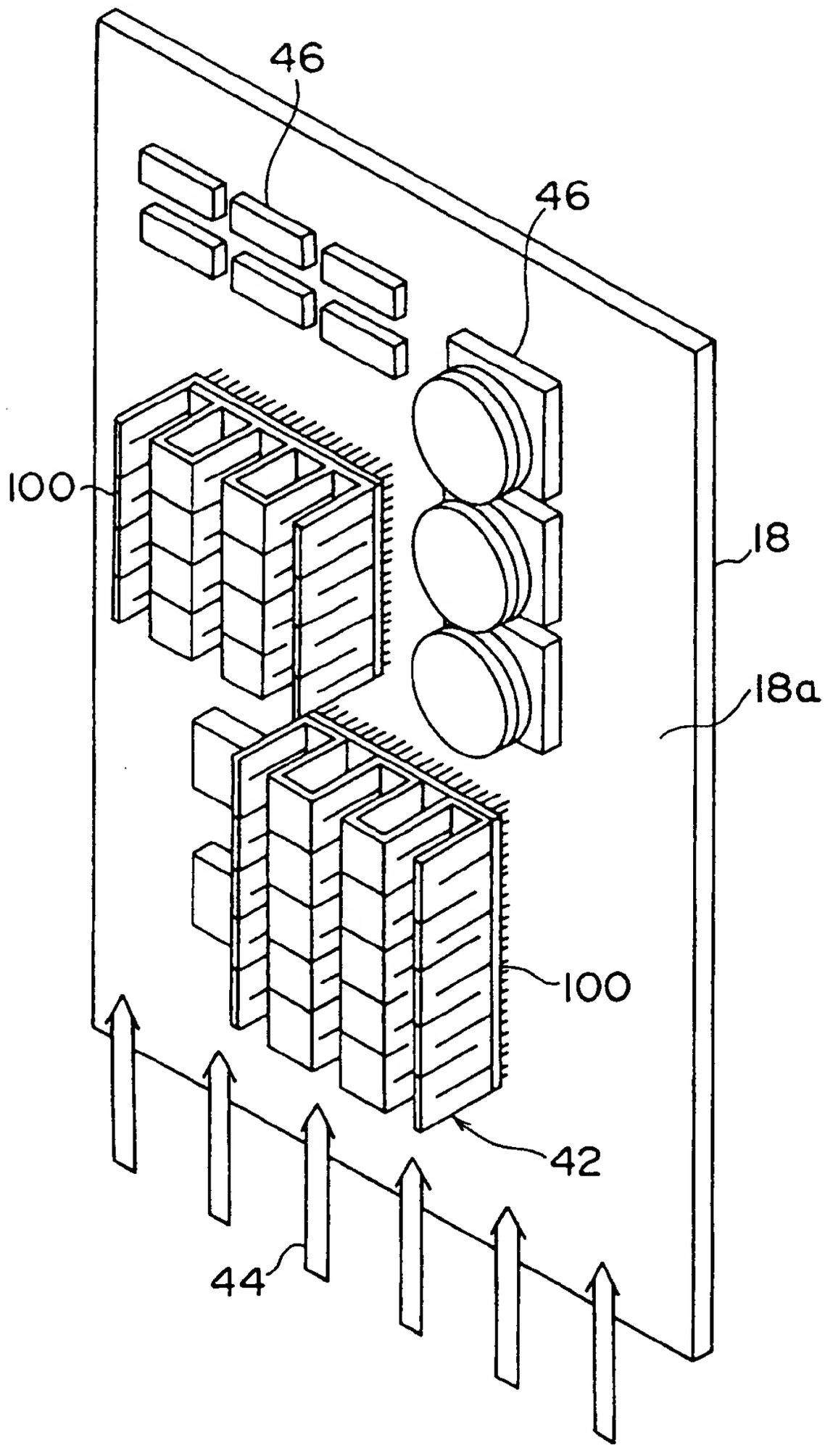


FIG. 8

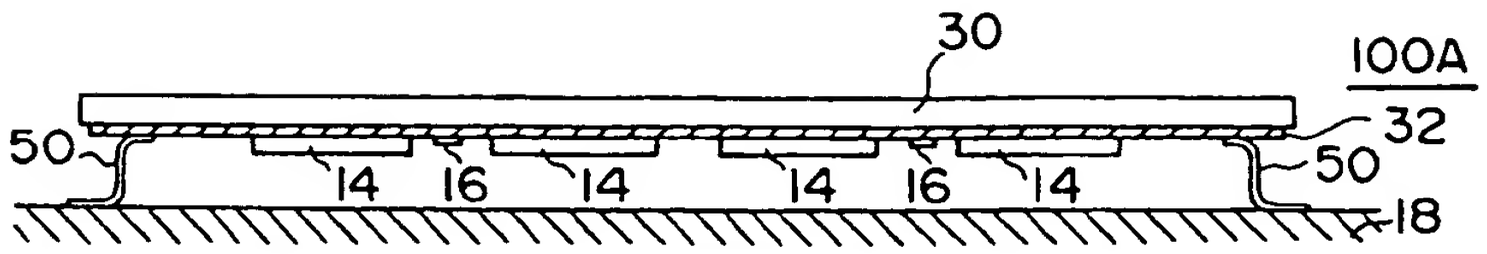


FIG. 9

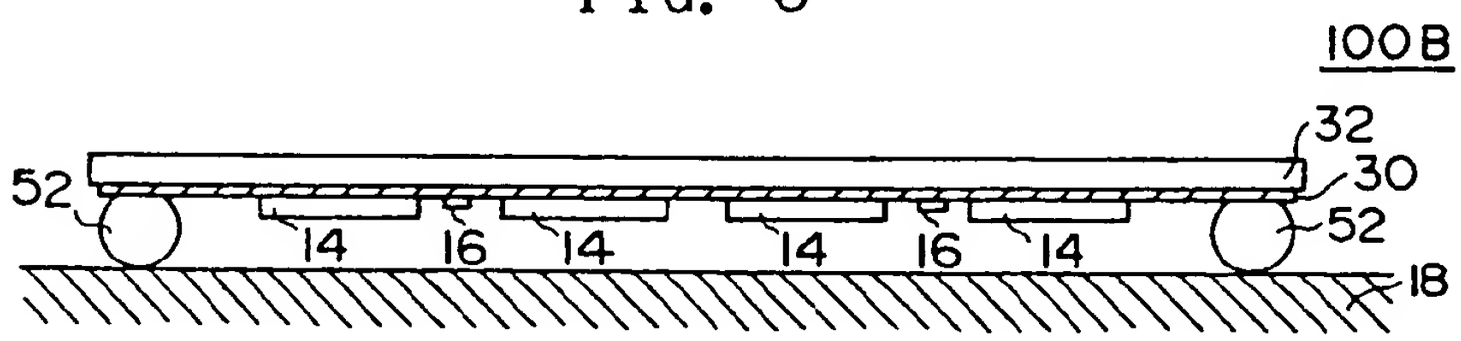


FIG. 10

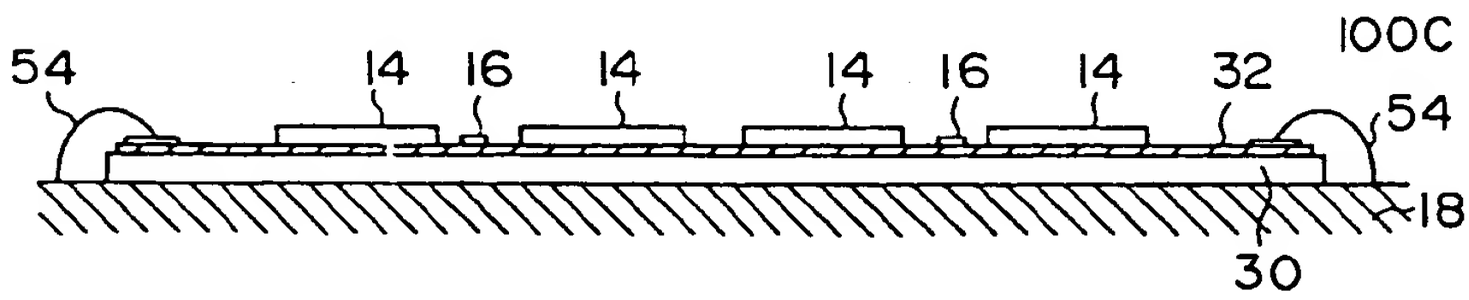


FIG. 11

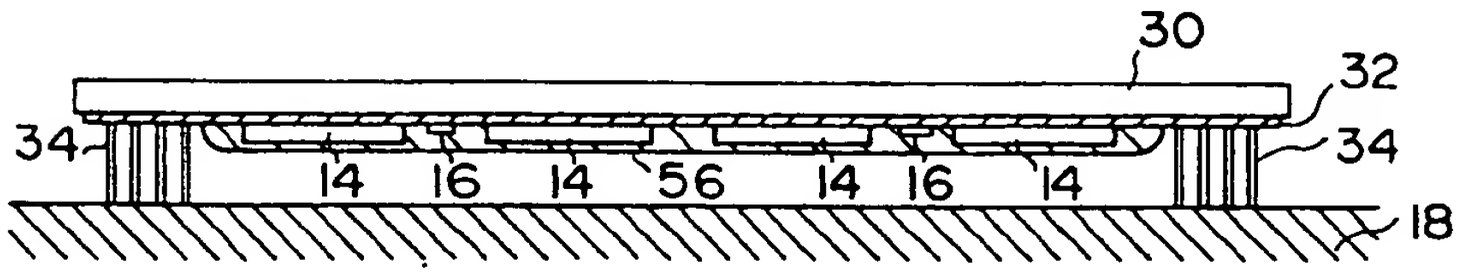


FIG. 12

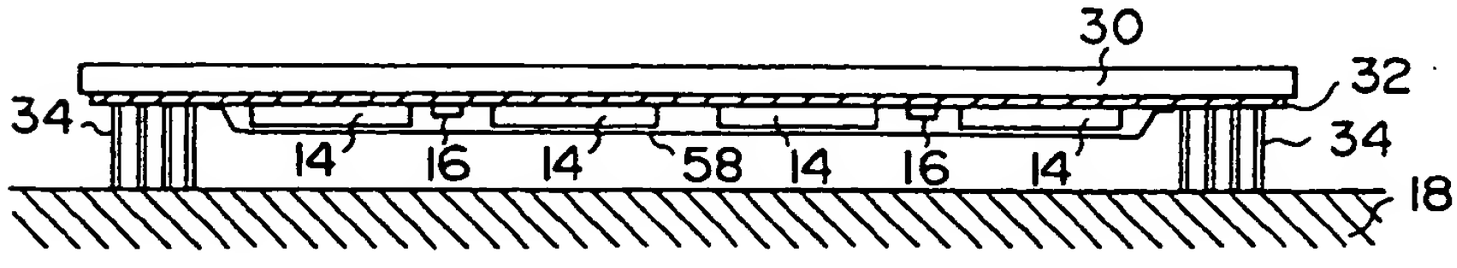


FIG. 13

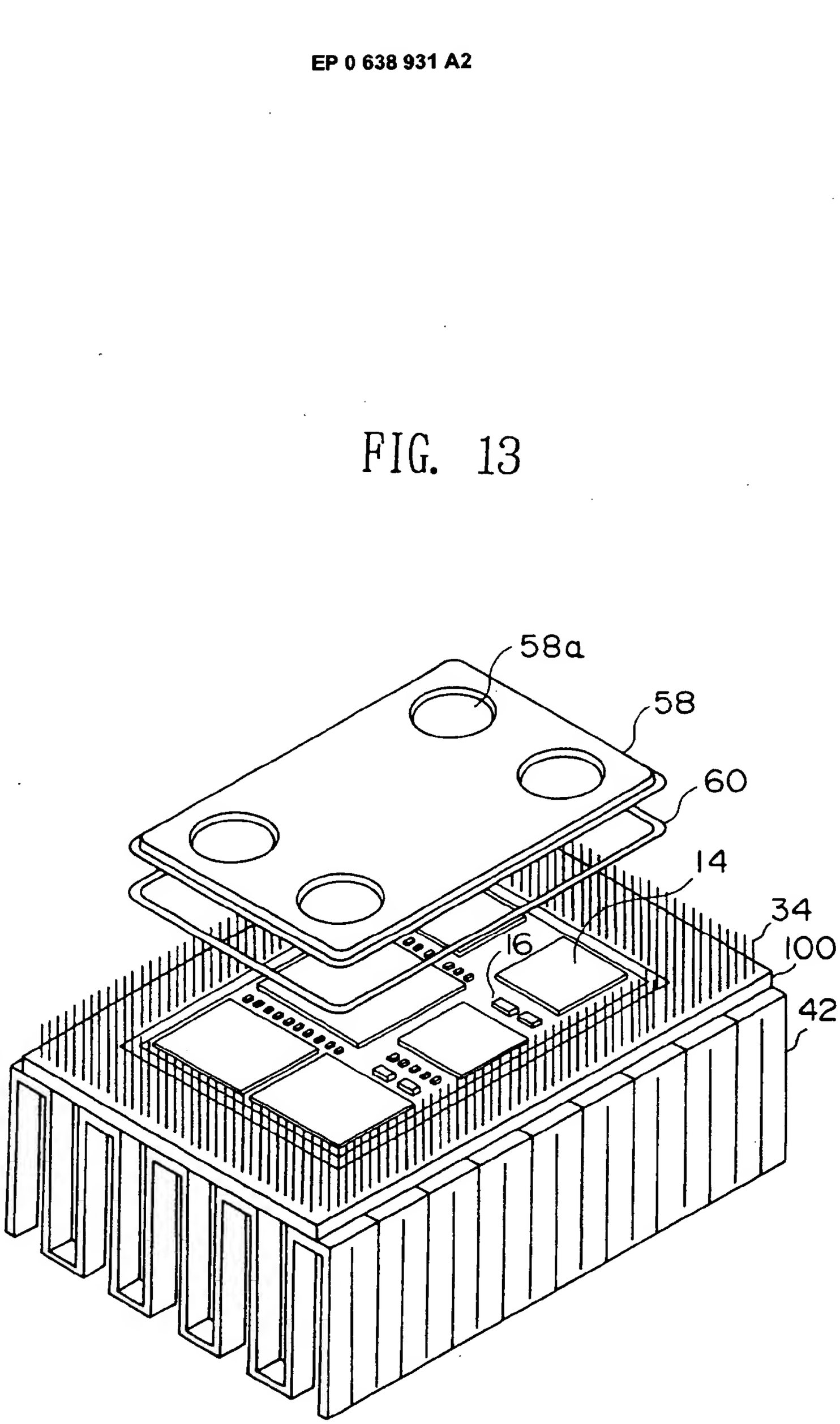


FIG. 14

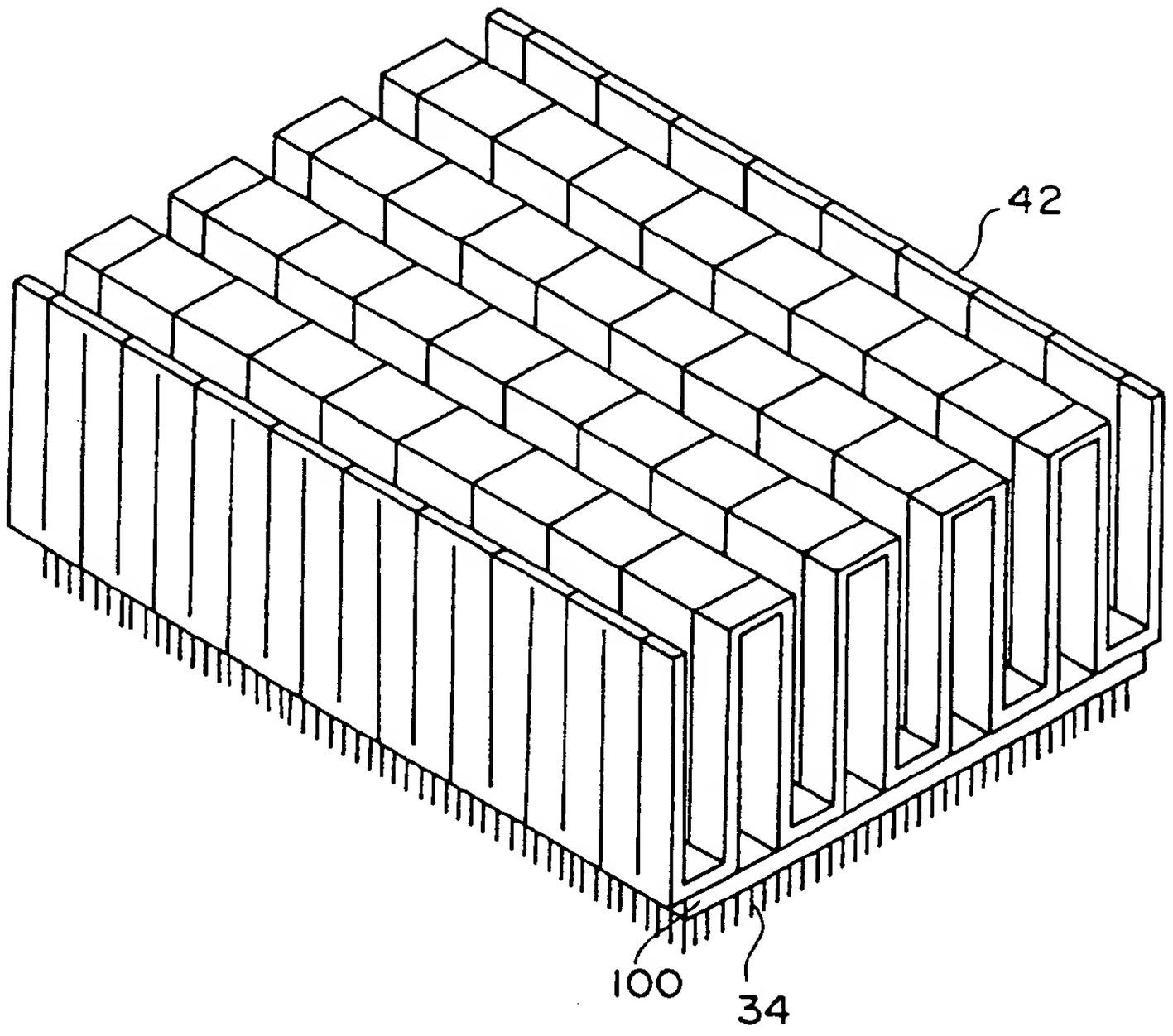
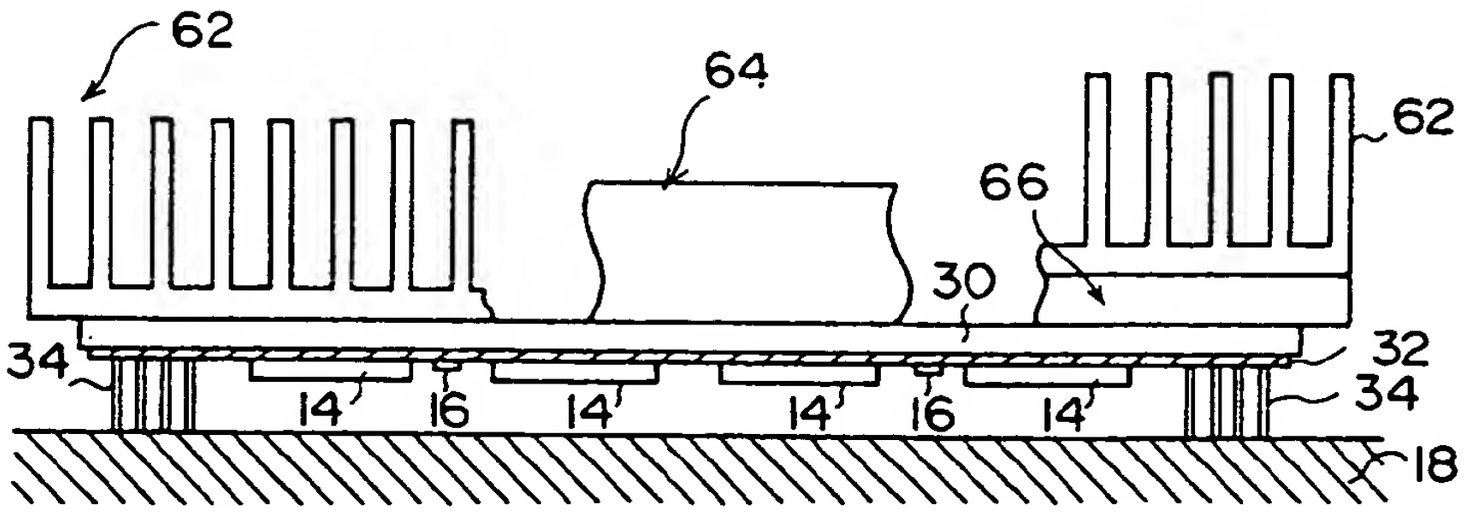


FIG. 15



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(54) **Multi-chip module.**

(57) A multi-chip module includes a base board (30), a thin-film multi-layer circuit board (32) which is provided on a first surface of the base board and has a multi-layer structure in which insulating layers and wiring conductors are stacked, circuit elements (32A-5) mounted on a main surface of the thin-film multi-layer circuit board, and terminals (34) which are attached to the main surface of the thin-film multilayer circuit board and electrically connect the wiring conductors to circuits formed on a wiring board on which the multi-chip module is mounted.

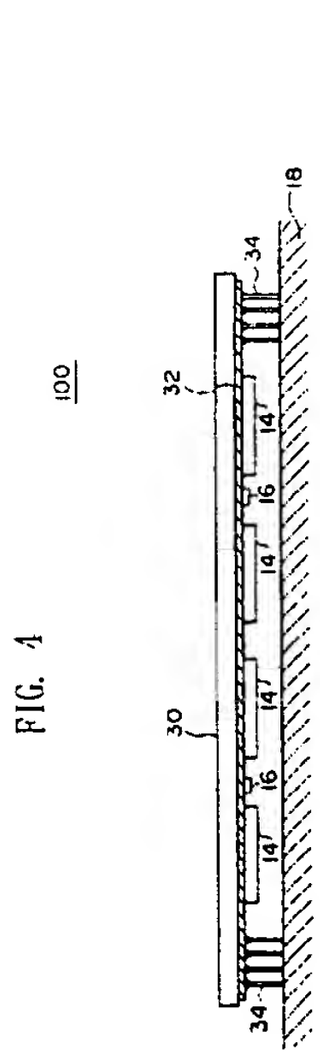

FIG. 1

EP 0 638 931 A3

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Application Number
EP 94 40 0928

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
Y	FR-A-2 557 755 (NEC) * the whole document * ---	1,2,4-7, 10-12	H01L23/538 H01L23/498 H01L25/065
Y	IEEE TRANSACTIONS ON COMPONENTS,HYBRIDS,AND MANUFACTURING TECHNOLOGY, vol.12, no.4, December 1989, NEW YORK US pages 658 - 662 S. SASAKI ET AL. 'A New Multichip Module Using a Copper Polyimide Multilayer Substrate' * the whole document * ---	1,2,4-7, 10-12	
Y	US-A-5 130 768 (WU ET AL.) * the whole document * ---	1,2,4-7, 10-12	
A	RESEARCH DISCLOSURE, no.326, June 1991, HAVANT GB page 401 'Low Profile Chip Package' abstr.nr. 326 31 * the whole document * ---	3	
A	1992 IEEE Multi-Chip Module Conference, MCMC-92, March 18-20, 1992, Santa Cruz, California, USA, pp.8-11, T. SUDO.: "Silicon-On-Silicon Technology for CMOS-Based Computer Systems" * figure 4 * ---	8	
A	EP-A-0 475 223 (NEC) * column 5, line 32 - column 8, line 22; figure 1 * --- -/--	8	

TECHNICAL FIELDS SEARCHED (Int.Cl.6)

H01L

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	8 March 1995	Prohaska, G

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Application Number
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DOCUMENTS CONSIDERED TO BE RELEVANT			
Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
A	EP-A-0 540 247 (IBM) * figures 1-3 *	9	
A	EP-A-0 509 825 (NEC) * abstract; figures 4-6 *	9	
A	EP-A-0 098 932 (IBM) * figures 5B,4B *	9	
			TECHNICAL FIELDS SEARCHED (Int.Cl.6)

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